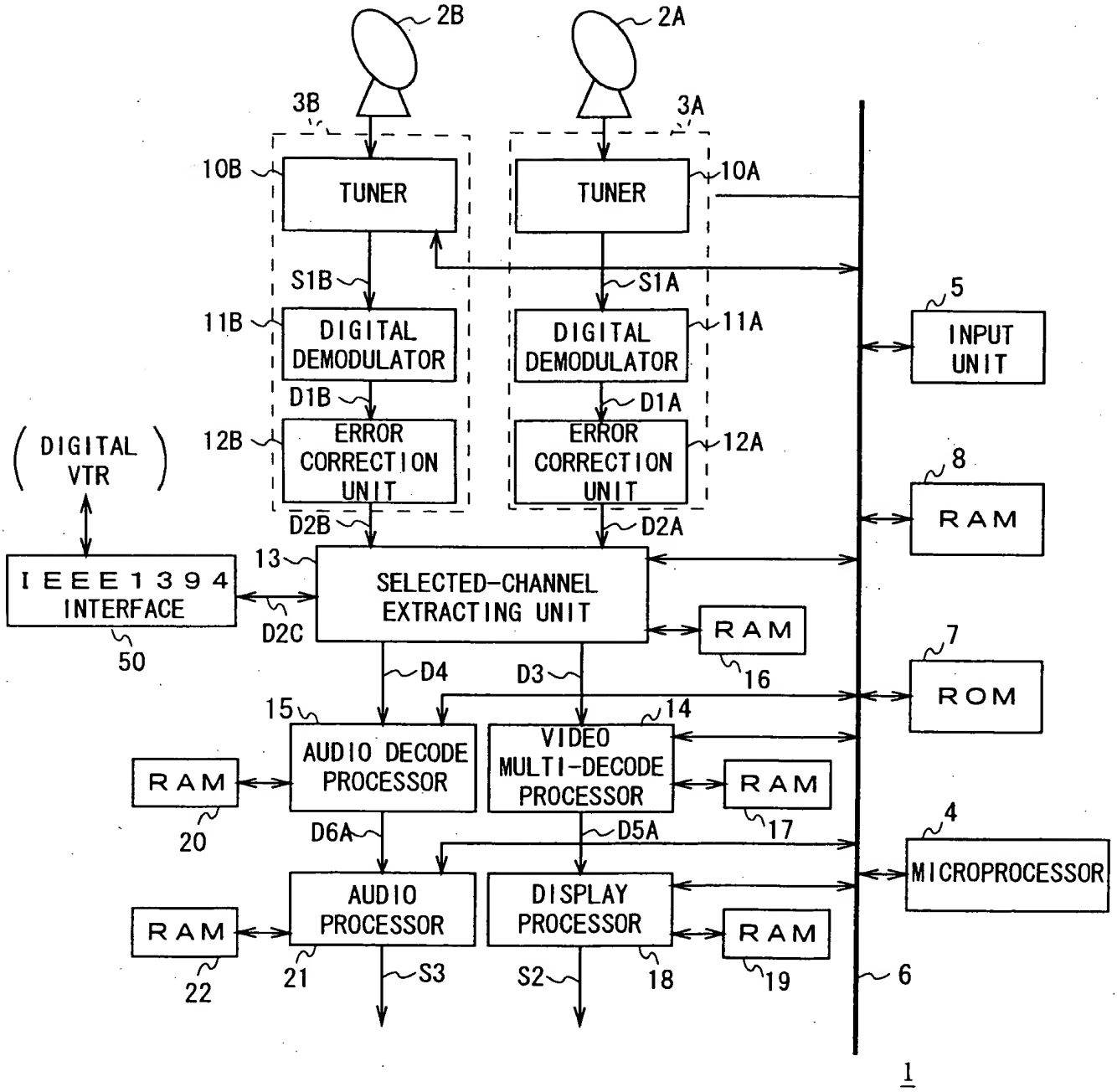
2B
2A
3B
3A
10B
TUNER
TUNER
10A
S1B
S1A
11B
DIGITAL DEMODULATOR
DIGITAL DEMODULATOR
11A
5
INPUT UNIT
D1B
D1A
DIGITAL VTR
12B
ERROR CORRECTION UNIT
ERROR CORRECTION UNIT
12A
8
RAM
D2B
D2A
13
IEEE1394 INTERFACE
SELECTED-CHANNEL EXTRACTING UNIT
D2C
RAM
16
50
7
D4
D3
ROM
15
14
AUDIO DECODE PROCESSOR
VIDEO MULTI-DECODE PROCESSOR
RAM
RAM
20
17
4
D6A
D5A
MICROPROCESSOR
AUDIO PROCESSOR
DISPLAY PROCESSOR
RAM
RAM
22
21
S3
S2
18
19
6
1

FIG. 1

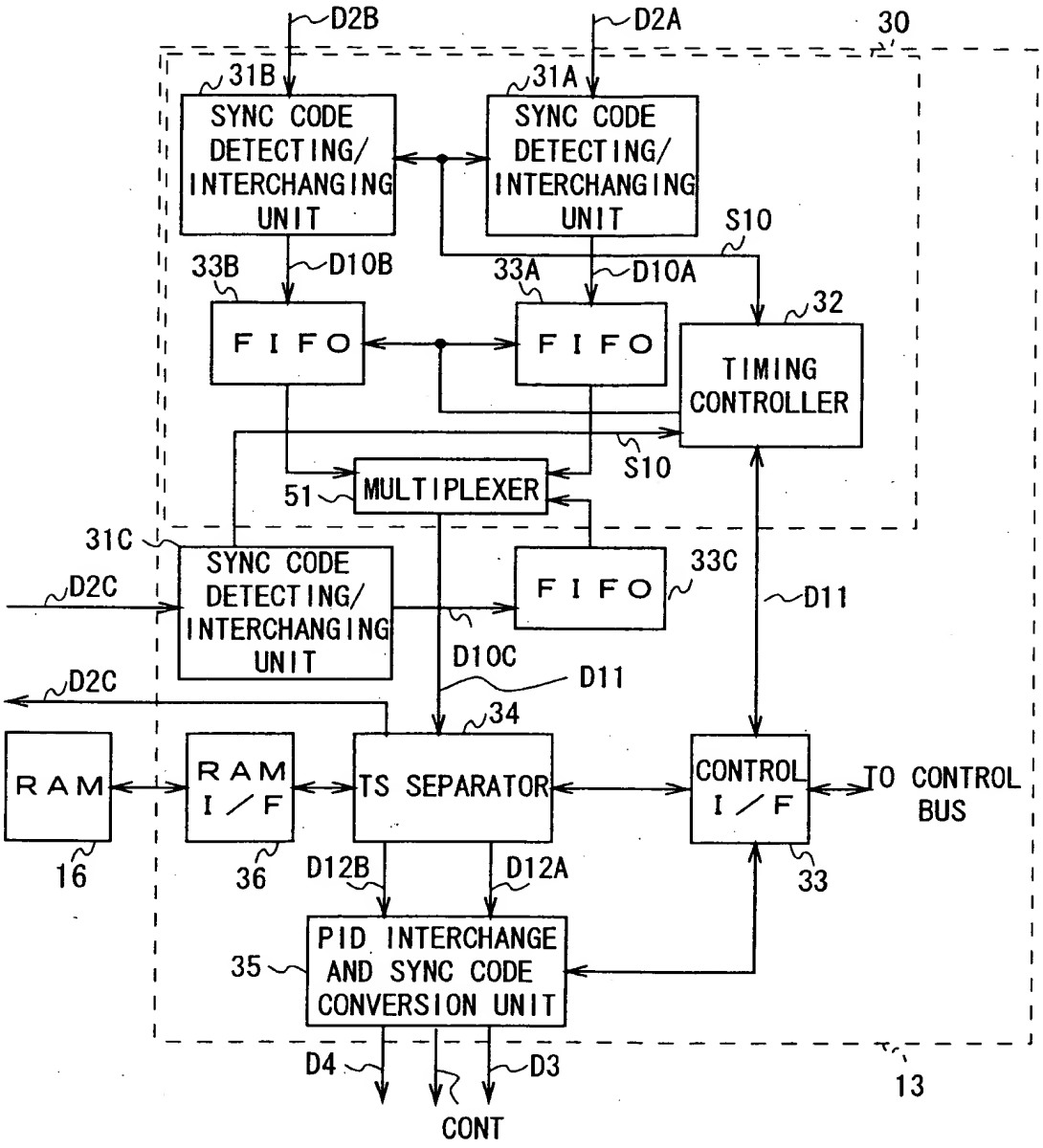
D2B
D2A
30
31B
31A
SYNC CODE DETECTING/ INTERCHANGING UNIT
SYNC CODE DETECTING/ INTERCHANGING UNIT
S10
33B
D10B
33A
D10A
32
F I F O
F I F O
TIMING CONTROLLER
S10
51
MULTIPLEXER
31C
SYNC CODE DETECTING/ INTERCHANGING UNIT
D2C
F I F O
33C
D11
D10C
D11
D2C
34
RAM
RAM I / F
TS SEPARATOR
CONTROL I / F
TO CONTROL BUS
16
36
D12B
D12A
33
PID INTERCHANGE AND SYNC CODE CONVERSION UNIT
35
D4
D3
13
CONT

FIG. 2

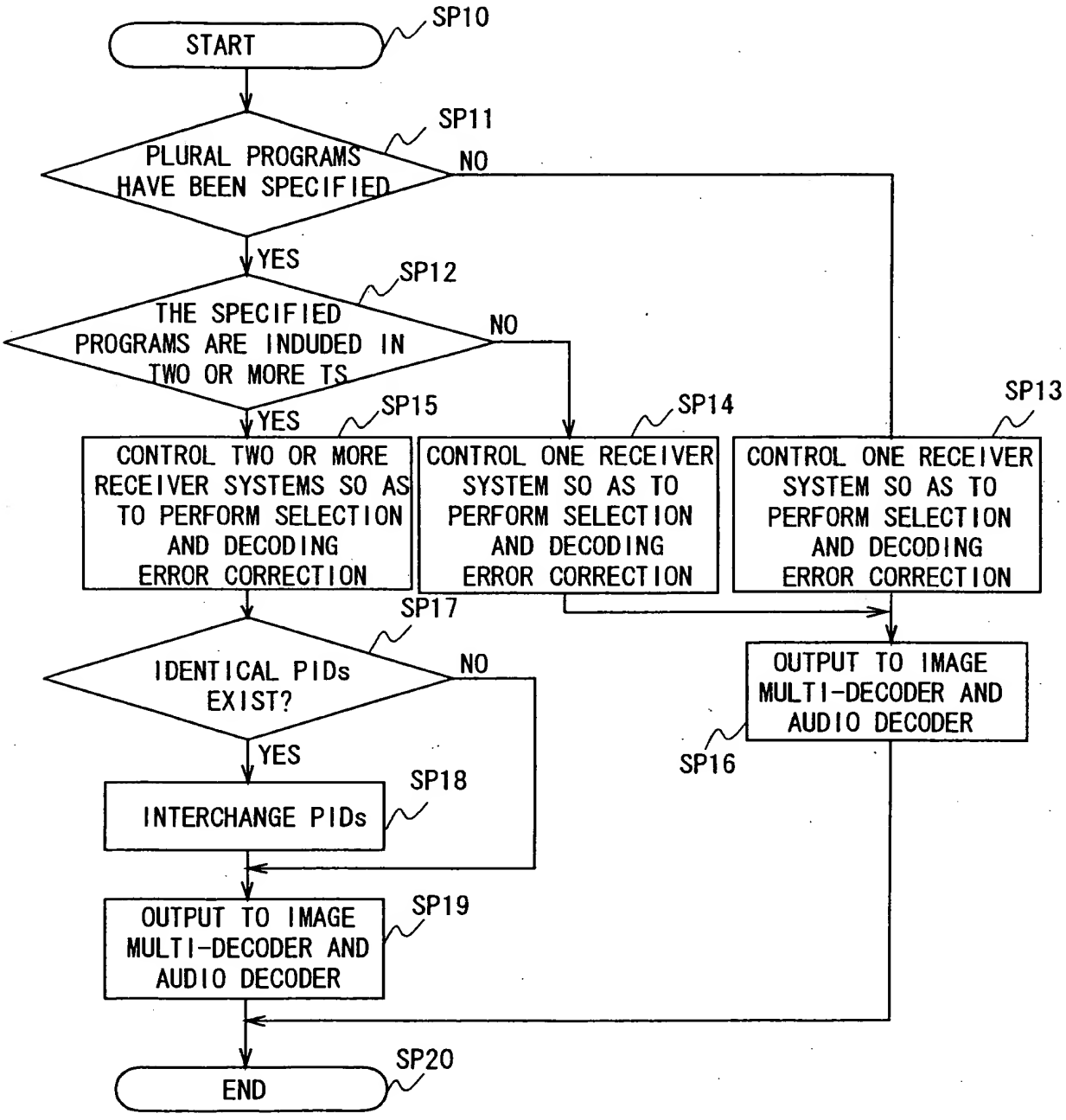
START
SP10
PLURAL PROGRAMS HAVE BEEN SPECIFIED
SP11
NO
YES
THE SPECIFIED PROGRAMS ARE INDUDED IN TWO OR MORE TS
SP12
NO
YES
CONTROL TWO OR MORE RECEIVER SYSTEMS SO AS TO PERFORM SELECTION AND DECODING ERROR CORRECTION
SP15
CONTROL ONE RECEIVER SYSTEM SO AS TO PERFORM SELECTION AND DECODING ERROR CORRECTION
SP14
CONTROL ONE RECEIVER SYSTEM SO AS TO PERFORM SELECTION AND DECODING ERROR CORRECTION
SP13
IDENTICAL PIDs EXIST?
SP17
NO
YES
INTERCHANGE PIDs
SP18
OUTPUT TO IMAGE MULTI-DECODER AND AUDIO DECODER
SP19
OUTPUT TO IMAGE MULTI-DECODER AND AUDIO DECODER
SP16
END
SP20

FIG. 3

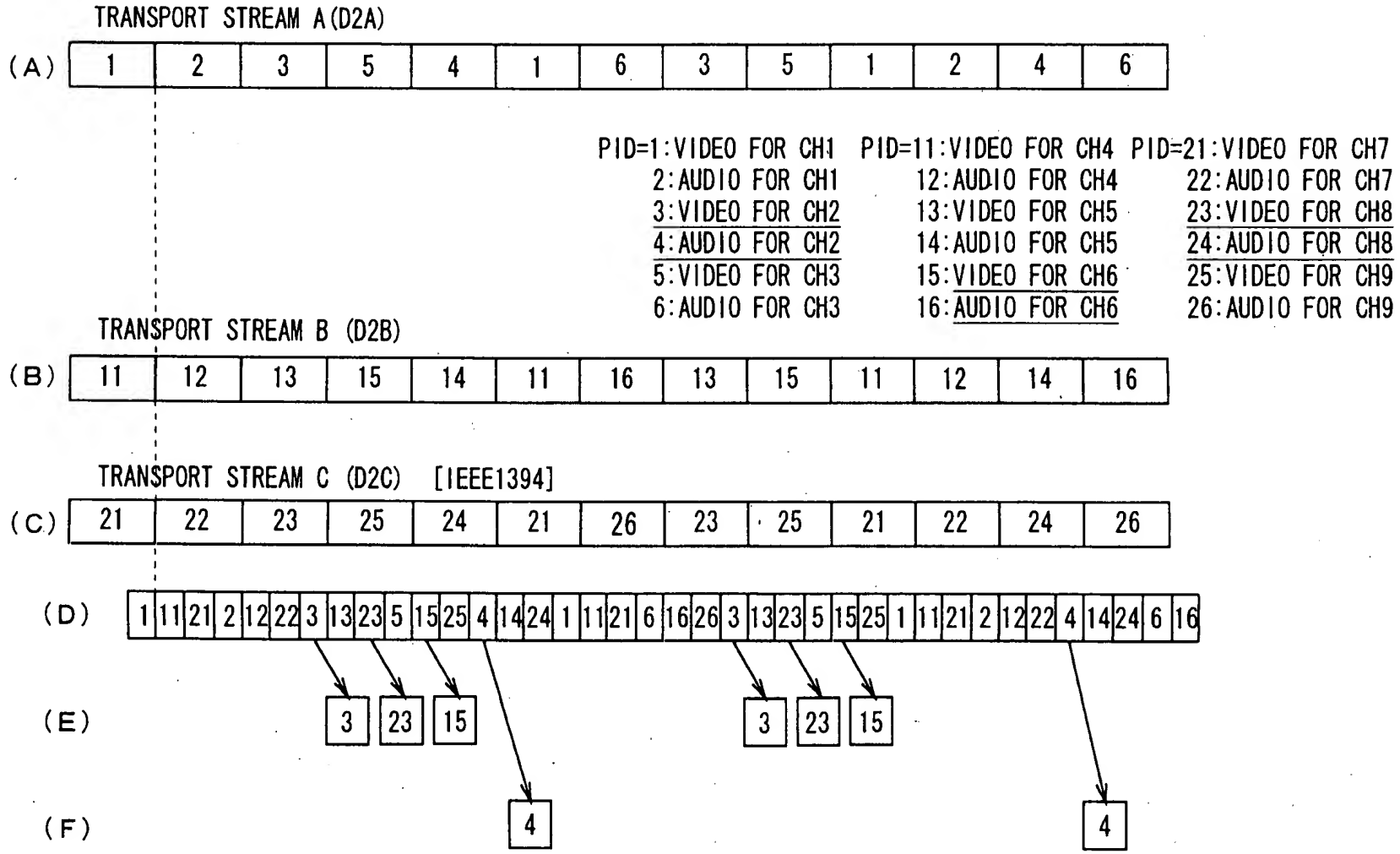
TRANSPORT STREAM A(D2A)
(A) 1 2 3 5 4 1 6 3 5 1 2 4 6
PID=1:VIDEO FOR CH1
2:AUDIO FOR CH1
3:VIDEO FOR CH2
4:AUDIO FOR CH2
5:VIDEO FOR CH3
6:AUDIO FOR CH3
PID=11:VIDEO FOR CH4
12:AUDIO FOR CH4
13:VIDEO FOR CH5
14:AUDIO FOR CH5
15:VIDEO FOR CH6
16:AUDIO FOR CH6
PID=21:VIDEO FOR CH7
22:AUDIO FOR CH7
23:VIDEO FOR CH8
24:AUDIO FOR CH8
25:VIDEO FOR CH9
26:AUDIO FOR CH9
TRANSPORT STREAM B (D2B)
(B) 11 12 13 15 14 11 16 13 15 11 12 14 16
TRANSPORT STREAM C (D2C) [IEEE1394]
(C) 21 22 23 25 24 21 26 23 25 21 22 24 26
(D) 1 11 21 2 12 22 3 13 23 5 15 25 4 14 24 1 11 21 6 16 26 3 13 23 5 15 25 1 11 21 2 12 22 4 14 24 6 16
(E) 3 23 15 3 23 15
(F) 4 4

FIG. 4

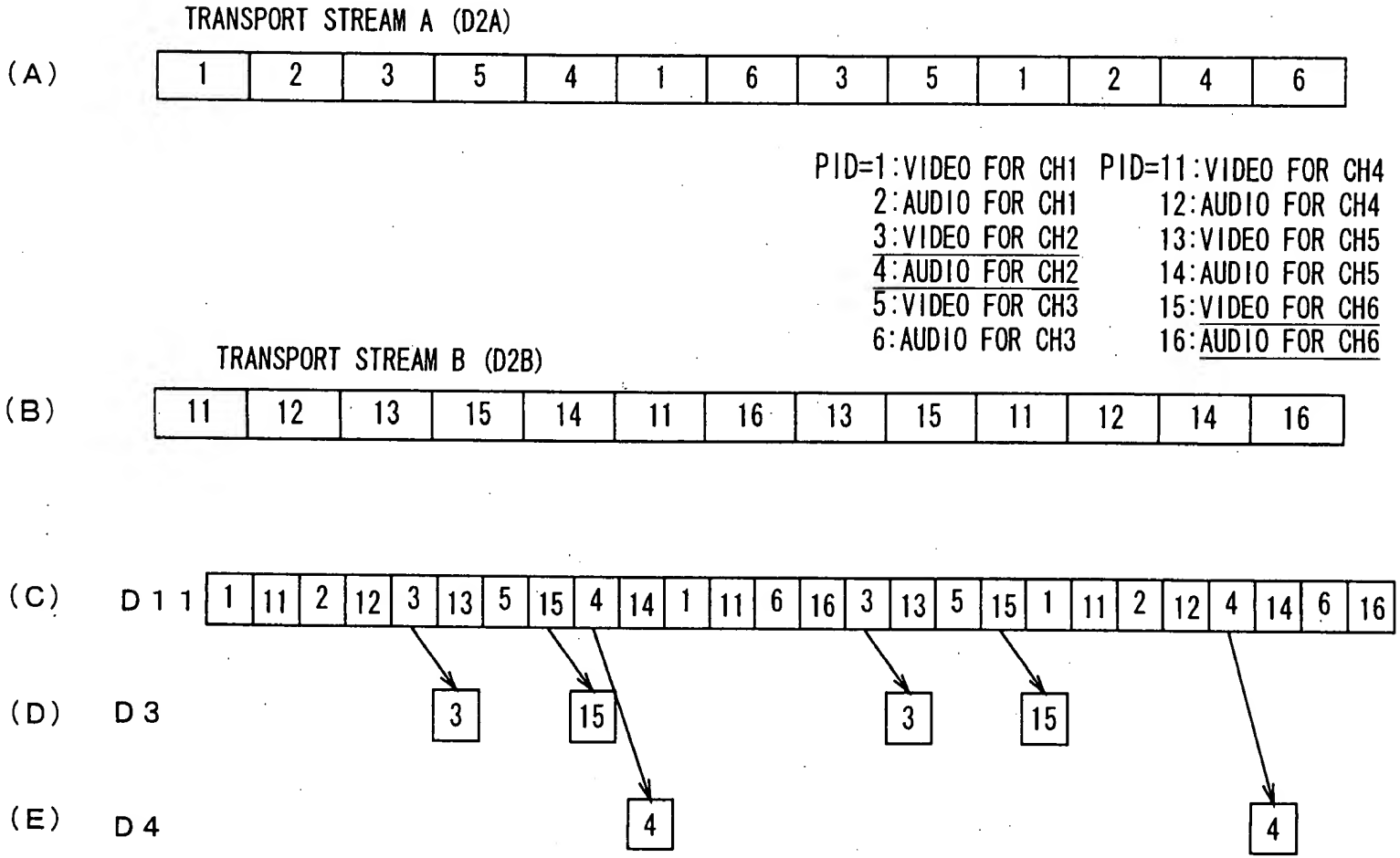
TRANSPORT STREAM A (D2A)
(A)
1 2 3 5 4 1 6 3 5 1 2 4 6
PID=1:VIDEO FOR CH1
2:AUDIO FOR CH1
3:VIDEO FOR CH2
4:AUDIO FOR CH2
5:VIDEO FOR CH3
6:AUDIO FOR CH3
PID=11:VIDEO FOR CH4
12:AUDIO FOR CH4
13:VIDEO FOR CH5
14:AUDIO FOR CH5
15:VIDEO FOR CH6
16:AUDIO FOR CH6
TRANSPORT STREAM B (D2B)
(B)
11 12 13 15 14 11 16 13 15 11 12 14 16
(C) D11
1 11 2 12 3 13 5 15 4 14 1 11 6 16 3 13 5 15 1 11 2 12 4 14 6 16
(D) D3
3 15 3 15
(E) D4
4 4

FIG. 5

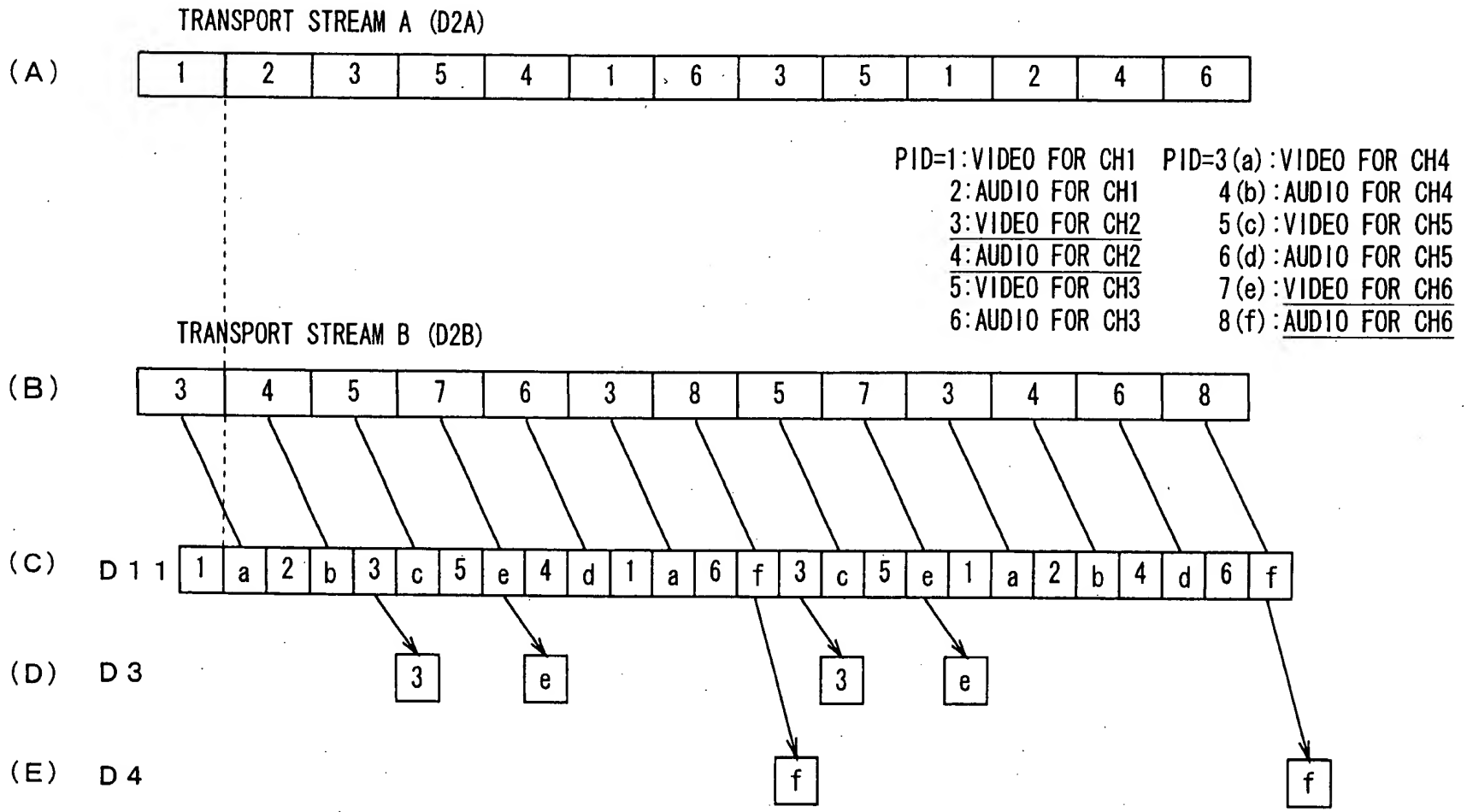
TRANSPORT STREAM A (D2A)
(A)
1 2 3 5 4 1 6 3 5 1 2 4 6
PID=1:VIDEO FOR CH1
2:AUDIO FOR CH1
3:VIDEO FOR CH2
4:AUDIO FOR CH2
5:VIDEO FOR CH3
6:AUDIO FOR CH3
PID=3(a):VIDEO FOR CH4
4(b):AUDIO FOR CH4
5(c):VIDEO FOR CH5
6(d):AUDIO FOR CH5
7(e):VIDEO FOR CH6
8(f):AUDIO FOR CH6
TRANSPORT STREAM B (D2B)
(B)
3 4 5 7 6 3 8 5 7 3 4 6 8
(C) D11
1 a 2 b 3 c 5 e 4 d 1 a 6 f 3 c 5 e 1 a 2 b 4 d 6 f
(D) D3
3 e 3 e
(E) D4
f f

FIG. 6

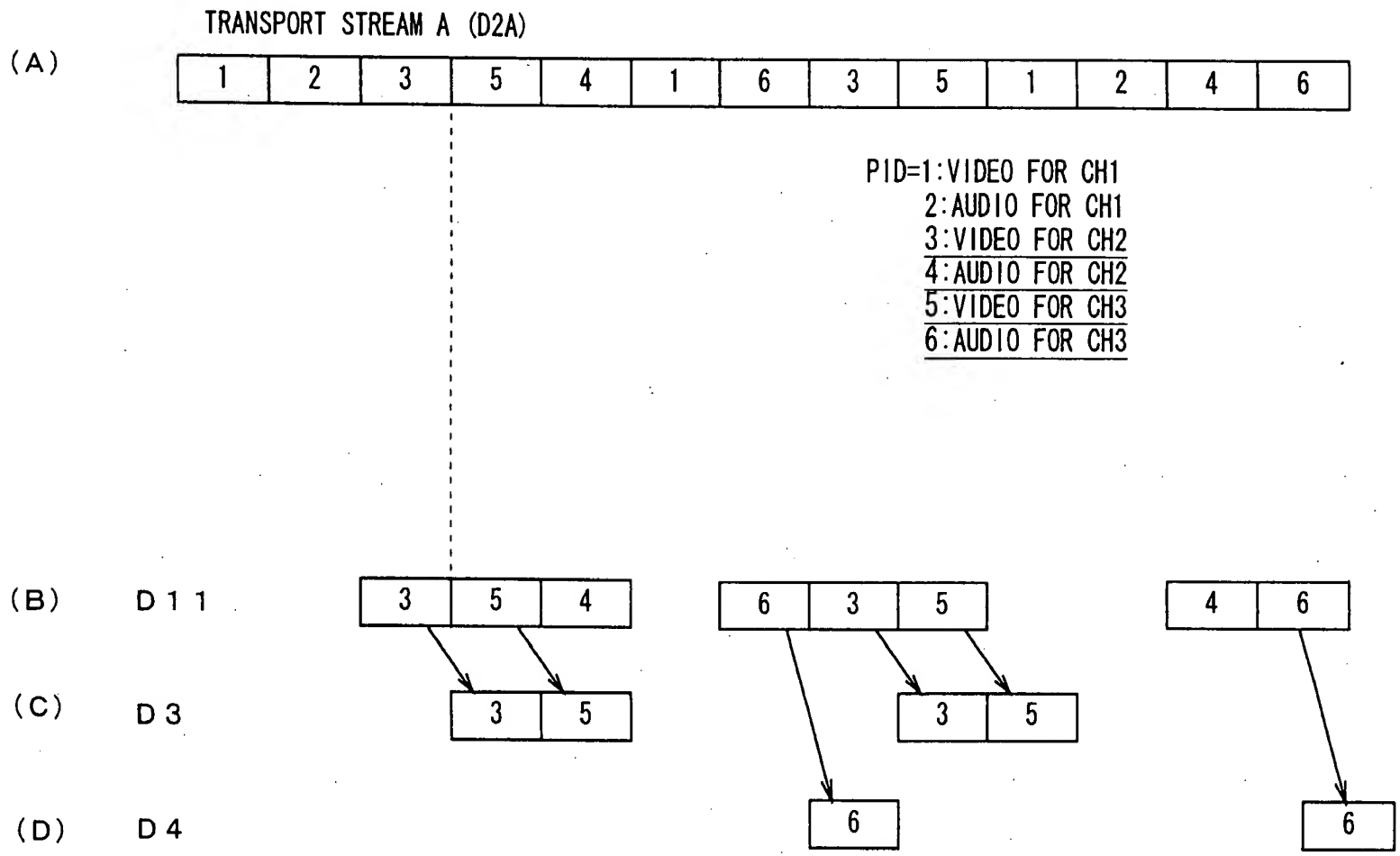
TRANSPORT STREAM A (D2A)
(A)
1 2 3 5 4 1 6 3 5 1 2 4 6
PID=1:VIDEO FOR CH1
2:AUDIO FOR CH1
3:VIDEO FOR CH2
4:AUDIO FOR CH2
5:VIDEO FOR CH3
6:AUDIO FOR CH3
(B) D11
3 5 4
6 3 5
4 6
(C) D3
3 5
3 5
(D) D4
6
6

FIG. 7

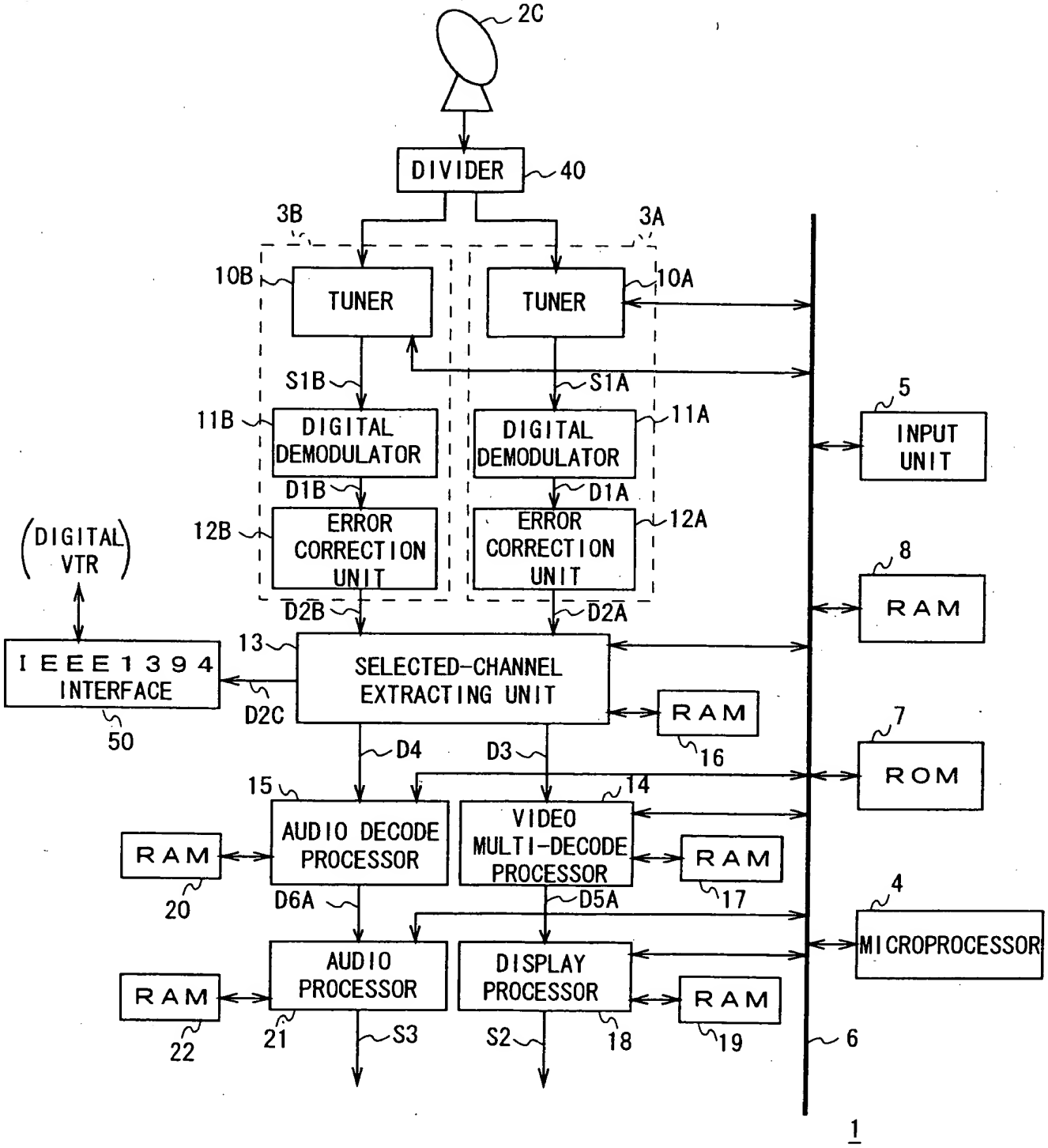
2C
DIVIDER
40
3B
3A
10B
TUNER
TUNER
10A
S1B
S1A
5
11B
DIGITAL DEMODULATOR
DIGITAL DEMODULATOR
11A
INPUT UNIT
D1B
D1A
(DIGITAL VTR)
12B
ERROR CORRECTION UNIT
ERROR CORRECTION UNIT
12A
8
RAM
D2B
D2A
13
IEEE1394 INTERFACE
SELECTED-CHANNEL EXTRACTING UNIT
RAM
D2C
50
16
7
D4
D3
ROM
15
14
AUDIO DECODE PROCESSOR
VIDEO MULTI-DECODE PROCESSOR
RAM
RAM
20
17
D6A
D5A
4
AUDIO PROCESSOR
DISPLAY PROCESSOR
MICROPROCESSOR
RAM
RAM
22
21
S3
S2
18
19
6
1

FIG. 8